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CERTIFICATE OF CORRECTION

PATENT NO. : 6,897,517
APPLICATION NO. : 10/603426
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INVENTOR(S) : Van Houdt et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

On page 1, at section (73) Assignees, after "Infineon" please insert --Technologies--.

On page 1, at section (73) Assignees, please delete "Munich" and insert therefore --Neubiberg--.

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(12) **United States Patent**
Van Houdt et al.

(10) **Patent No.: US 6,897,517 B2**
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(54) **MULTIBIT NON-VOLATILE MEMORY AND METHOD**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **10/603,426**

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Related U.S. Application Data

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(51) **Int. Cl.**[7] **H01L 29/788**

(52) **U.S. Cl.** **257/315**; 257/239; 257/261; 257/316; 257/317; 257/320; 257/321; 438/201; 438/211; 438/216; 438/241; 438/257; 438/260

(58) **Field of Search** 257/239, 261, 257/298, 315–326; 438/201, 211, 216, 241, 257–258, 260–266, 591, 593

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(57) **ABSTRACT**

A memory is described having a semiconductor substrate of a first conductivity type, a first and a second junction region of a second conductivity type, whereby said first and said second junction region are part of respectively a first and a second bitline. A select gate is provided which is part of a wordline running perpendicular to said first and said second bitline.

Read, write and erase functions for each cell make use of only two polysilicon layers which simplifies manufacture and each memory cell has at least two locations for storing a charge representing at least one bit.

13 Claims, 21 Drawing Sheets